REMARKS

Claims 1-21 are all the claims pending in the application. Claims 22-41 have been canceled as being directed to a different invention. Claims 2-4 stand objected to only as being dependent upon a rejected base claim, and would be allowable if rewritten in independent form to include all the limitations of the base claim and any intervening claims. Claim 2 has been rewritten in independent form to place claims 2-4 for in condition for immediate allowance.

Claims 1 and 5-7 stand rejected on prior art grounds. Applicants respectfully traverse this rejection based on the following discussion.

I. The Prior Art Rejections

Claims 1 and 5-7 stand rejected under 35 U.S.C. §102(e) as being anticipated by Cleeves et al., (6,580,124). Applicants respectfully traverse this rejection principally because Cleeves does not teach or suggest that "said back gate conductors and said front gate conductors are alternatively interdigitated between channel regions of said fin structures such that each of said channel regions has a back gate conductor on one side of each fin structure and a front gate conductor on the other side of said fin structure" as defined by independent claim 1. Therefore, as explained in greater detail below, it is Applicants position that independent claim 1, and dependent claims 5-7, are patentable over Cleeves.

More specifically, the invention produces a split-gate fin-type field effect transistor (FinFET) that has parallel fin structures. Each of the fin structures has a source region at one end, a drain region at the other end, and a channel region in the middle portion. Back gate conductors are positioned between channel regions of alternating pairs of the fin structures and front gate conductors are positioned between channel regions of opposite alternating pairs of the fin structures. Thus, the back gate conductors and the front gate conductors are alternatively interdigitated between channel regions of the fin structures. Also, each of the channel regions has a back gate conductor on one side of each fin structure and a front gate conductor on the

other side of the fin structure. The front gate conductors are positioned adjacent to outer sides of channel regions of end fin structures of the split gate FinFET. There are also gate oxides between the back and front gate conductors and the channel regions.

The invention solves a number of problems associated with SOI structures by providing a multiple-fin FinFET structure that has self-aligned front and back gates. The channel regions in SOI structures are placed above insulators and are therefore floating. Thus, it is important to provide a back gate in SOI structures in order to control the voltage level of the channel region which provides threshold voltage of the transistor. The invention utilizes SOI fin channel regions that are electrically insulated above an insulating layer. In order to control the voltage of the fin channel regions, the back gate is placed on one side of the fin channel regions. The front gate is positioned on the other side of the fin channel regions.

The front and back gates are patterned simultaneously (e.g., in the same process using the same mask) which provides that the front and back gates will be naturally (automatically) aligned with each other. The same (or similar) mask that is used to pattern the front and back gate is also used to control the doping of the source/drain regions (wherein the channel region is protected) which also allows the gates to be easily and accurately aligned with the source/drain regions.

Thus, this method provides a structure that has front and back gates that are self-aligned with one another and with the source/drain regions. This allows the back gate to control the threshold voltage of transistors even for structures that utilize multiple fins. With such self-alignment, the power and delay is substantially decreased and the density of transistors is increased, leading to reduced costs.

To the contrary, Cleeves discloses a silicon channel body having a first and second channel surface. In Cleeves, a charge storage medium is adjacent to the first channel surface and a second charge storage medium is adjacent to the second channel surface. A first control gate is adjacent to the first charge storage medium adjacent to the first channel surface and a second control gate is adjacent to the second charge storage medium adjacent to the second surface. In addition, Cleeves discloses a transistor that has a source, a channel, a drain, and a plurality of gates where the channel current flows vertically between the source and drain. Also, in Cleeves,

a memory element is formed using a transistor that has a read current that flows in a direction perpendicular to a substrate in or over the transistor. This transistor has a charge storage medium for storing its state. Multiple control gates address the transistor.

Therefore, it is applicants position that Cleeves does not teach or suggest that "said back gate conductors and said front gate conductors are alternatively interdigitated between channel regions of said fin structures and such that each of said channel regions has a back gate conductor on one side of each fin structure and a front gate conductor on the other side of said fin structure" as defined by independent claim 1. Therefore, Applicants submit that independent claim 1, and dependent claims 5-7, are patentable over Cleeves. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdrawn this rejection.

II. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1-21, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

10/605,544

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: 10/22/04

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